1 Pixel System General

The pixel system is the part of the tracking system that is closest to the interaction point. It contributes precise tracking points in r-phi and z and therefore is responsible for a small impact parameter resolution that is important for a good secondary vertex reconstruction. With a pixel cell size of $150 \times 100 \mu m^2$ an emphasis has been made to achieve similar track resolution in r-phi and z-direction. Through this a 3D vertex reconstruction in space is possible, which will be important for secondary vertices with low track multiplicity. The pixel system has a zero-suppressed read out scheme with analog pulse height readout. This improves the position resolution due to charge sharing and helps to separate signal and noise hits as well as to identify large hit clusters from overlapping tracks. The pixel detector covers a pseudo rapidity range -2.5$< \eta <$2.5, matching the acceptance of the central tracker. The pixel detector is essential for the reconstruction of secondary vertices from b and tau decays, and forming seed tracks for the outer track reconstruction and L2/L3 triggering. It consists of three barrel layers (BPix) with two end-cap disks (FPix).The 53 cm long BPix layers will be located at mean radii of 4.4, 7.3 and 10.2 cm. The FPix disks extending from $\sim$6 to 15 cm in radius, will be placed on each side at z=$\pm$34.5 and z=$\pm$46.5cm. Bpix (Fpix) contain 48 million (18 million) pixels covering a total area of 0.78 (0.28) m^2. The arrangement of the 3 barrel layers and the forward pixel disks on each side gives 3 tracking points over almost full eta-range. Figure **??** shows the geometric arrangement and the hit coverage as a function of pseudorapidity η. In the high eta region the 2 disk points are combined with the lowest possible radius point from the 4.4 cm barrel layer. The vicinity to the interaction point also implies a very high track rate and particle fluencies that requires a radiation tolerant design. For the sensor this led to an n+ pixel on n-substrate detector design that allows partial depleted operation even at very high particle fluencies. For the barrel layers the drift of the electrons to the collecting pixel implant is perpendicular to the 4T magnetic field of CMS. The resulting Lorentz drift leads to charge spreading of the collected signal charge over more than one pixel. With the analog pulse height being read out a charge interpolation allows to achieve a spatial resolution in the range of 10-12μm. The forward detectors are tilted at 20° in a turbine-like geometry to induce charge sharing so that the drift direction is not parallel to the magnetic field. A position resolution of approximately 10 μm in both directions can be achieved with charge sharing between neighboring pixels. The reduction in the depletion depth or the increase in bias voltage will lead to a reduction of charge sharing and therefore a degradation of the spatial resolution with radiation damage. In order to allow a replacement of the innermost layers the mechanics and the cabling of the pixel system has been designed such to allow a yearly access if needed. At full LHC luminosity we expect the innermost layer to stay operational for at least 2 years. The 3 layers barrel mechanics as well as the forward disks is completely divided into a left and right half. This is required to allow installation along the beam pipe and to pass beyond the beam pipe support wires at z=$\pm$ xxx cm. The 6 individual mechanical pieces are referenced to each other through precise machined rails inside the TIB cylinder. Power, cooling, the optical controls as well as the optical read out lines are brought to the detector through supply tube shells. In case of the barrel pixel system the supply tubes have a flexible connection that needs to bend by a few degrees during insertion following the slightly curved rails around the beam pipe support ring. Pixel system is inserted as the last subdetector of CMS after the silicon tracker has been installed and after the central section of the beam pipe has been installed and baked out.

2 Sensor description

2.1 Technological choices

The sensors for the CMS-pixel detector adopt the so called "n-in-n" concept: The pixels consist of high dose n-implants introduced into a high resistive n-substrate. The rectifying pn-junction is placed on the back side of the sensor surrounded by a multi guard ring structure. Despite of the higher costs due to the double sided processing this concept was chosen as the collection of electrons assure a high signal charge at moderate bias voltages (< 600 V) after high hadron fluences. Further the double sided processing allows a guard ring scheme keeping all sensor edges at ground potential.

The isoloation technique aplied for the regions between the piel electrodes was developed in close collaboration with the sensor vendors. Open p-stops [5] were chosen for the disks and moderated p-spray [2] for the barrel. Both types of sensors showed sufficient radiation hardness during an extensive qualification procedure including several test beams [4, 3].

2.2 Disk Sensors

The disk sensors use the p-stop technique for interpixel isolation. To maximize the charge collection efficiency and minimize the pixel capacitance within the design rules of the vendor a width of 8μm for the p-stop rings and

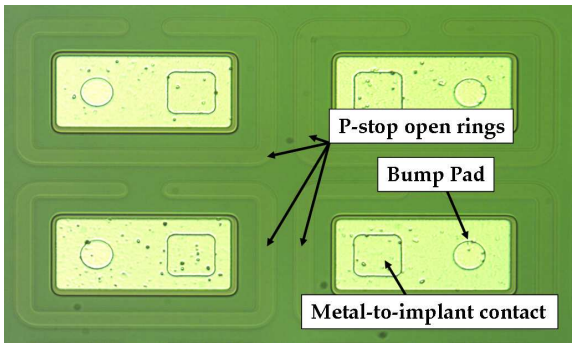

Figure 1: Picture of four pixels in the same double column for a forward pixel sensor.

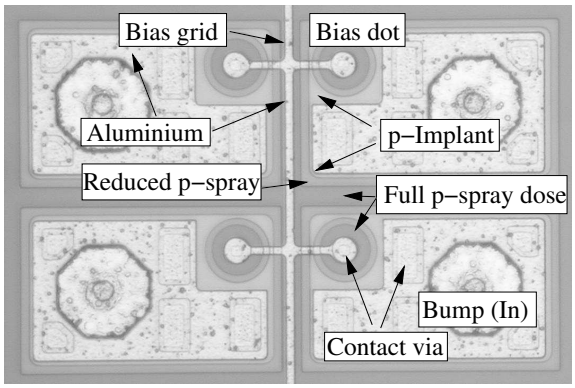

Figure 2: Photograph of four pixel cells. The Indium bumps are already deposited but not yet reflown.

a distance of 12μm between implants was chosen. Figure 1 shows a photograph of 4 pixel cells. The open ring p-stops, the bump-bonding pad and the contact between the aluminum and the implanted collecting electrode are highlighted.

The opening on the p-stop rings provides a low resistance path untill full depletion is reached to allow IV carachterization of the sensor on wafer and a high resistance path when the sensor is overdepleted (10-20 V overdepletion) to assure interpixel isolation.

The process used by Sintef [6] is completely symmetric with five photolitographic steps on each side to minimize the mechanical stress on the silicon substrate and the potential bowing of the diced sensors.

The sensor were all fabricated in 2005 on 4 inch wafers. The depletion voltage is 45-50 V and the leakage current is less than 10nA per cm^2. The 7 different sensor tiles needed to populate a disk blade, ranging from 1×2 ROCs to 2×5 ROCs are implemented on a single wafer.

A production yield higher than 90% has been achieved and 150 good sensor for each of the seven flavors are available to the project for module assembly.

2.3 Barrel Sensors

The sensors for the pixel barrel use the moderated p-spray technique for interpixel isolation. A photograph of four pixels in a barrel sensor is shown in Fig. 2. Most area of a pixel is covered with the collecting electrode formed by the n-implant. The gap between the n-implants is kept small (20 μm) to provide a homogeneious drift field which leads to a relatively high capacitance of the order of 80-100 fF per pixel.

In one corner of each pixel the so called *bias dot* is visible. They provide a high resistive punch-through connection to all pixels which allows on-wafer current-voltage (IV) measurements which are important to exclude faulty sensors from the module production.

The dark "frame" around the pixel implants visible in Fig. 2 indicates the opening in the nitride covering the thermal oxide. In this region the p-spray dose reaches the full level. Close to the lateral pn-junction between the pixel implant and the p-sprayed inter-pixel region the boron dose is reduced.

The sensor shown in Fig. 2 has undergone the bump deposition process. The Indium bumps are visible as roughly

$50\ \mu$m wide octogons.

The sensors are processed on n-doped DOFZ-silicon [1] with $\langle 111 \rangle$ orientation and a resistivity of about $3.7\ \mathrm{k\Omega cm}$ (after processing). This leads to a full depletion voltage of 50-60 V of the $285\ \mu$m thick sensors. All wafers for the production of the barrel sensors come from the same silicon ingot to provide the best possible homogeneity of all material parameters.

The pixel barrel requires two different sensor geometries, 708 full (2×8 ROCs) and 96 half modules (1×8 ROCs). They were processed by CiS [7] in 2005 and 2006 using two different mask sets.

3 Pixel Detector Readout

3.1 System Overview

The pixel readout and control system [8] consists of three independent parts: the detector front end, the pixel front end controller (pFEC) and the pixel front end driver (pxFED). Figure 3 shows a sketch of the system.
The front end consists of a Token Bit Manager (TBM) chip which controls several readout chips (ROCs). The TBM contains a communication component called the HUB. The pFEC sends the 40MHz clock and fast control signals (e.g. trigger, reset) to the front end and programs all front end devices. The pxFED receives data from the front end, digitizes it, formats it and sends it to the CMS-DAQ event builder. pFEC and pxFED are VME modules located in the electronics room and are connected to the front end through 40 MHz optical links. The various components are described in the following sections.

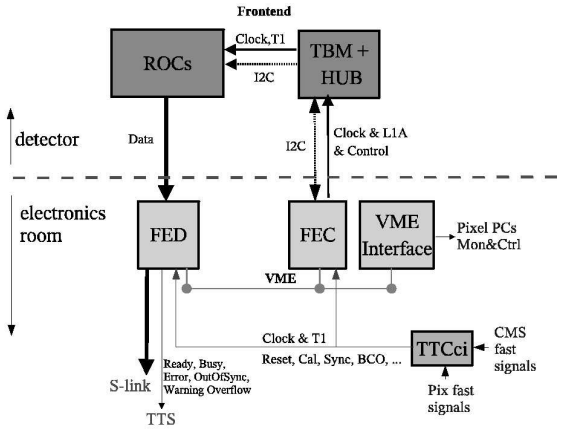

Figure 3: Block diagram of the pixel control and readout system.

3.2 Readout Chip

Sensor signals are read out by readout chips (ROC) bump bonded to the sensors. A ROC is a full custom ASIC fabricated in a commercial 0.25μm 5 metal layer CMOS process and contains 52×80 pixels [9]. Its main purposes are:

- Amplification and buffering of the charge signal from the sensor.
- Zero suppression in the pixel unit cell. Only signals above a certain threshold will be read out. This threshold can be adjusted individually for each pixel by means of four trim bits. The trim bits have a capacitive protection against single event upset (SEU), which has shown to reduce SEU by 2 orders of magnitude [9]. The mean threshold dispersion after trimming at T=-10°C is 90 electron equivalents with a noise of 170 electrons.
- Level 1 trigger verification. Hit information without a corresponding L1 trigger is abandoned.
- Sending hit information and some limited configuration data (analog value of last addressed DAC) to the TBM chip. Pixel addresses are transferred as 6 level analog encoded digital within 5 clock cycles (125ns) while the pulse height information is truly analog.

- Adjusting various voltage levels, currents and offsets in order to compensate for chip-to-chip variations in the CMOS device parameters. There are a total of 29 DACs on the chip.

The ROC needs two supply voltages of 1.5V and 2.5V. There are 6 on chip voltage regulators. This makes it possible to operate the detector without voltage regulator boards inside the CMS detector, improves AC power noise rejection and strongly reduces intermodule cross-talk. The total power consumption is 120mW per chip or 30μW per pixel. The temperature can be measured with an on-chip temperature sensor. The ROC is controlled through a modified I^2C interface running at 40 MHz. The configuration data can be downloaded without stopping data taking.
There are a few architecture inherent data loss mechanisms. The particle detection efficiency has been measured in a high rate pion beam. It is in fairly good agreement with expectations an reaches 0.8%, 1.2% and 3.8% respectively for the three layers at a luminosity of $10^{34}\mathrm{s}^{-1}\mathrm{cm}^{-2}$ and 100kHz L1 trigger rate.

3.3 Token Bit Manager Chip

The TBM ([10]) controls the readout of a group of pixel ROCs. The TBM is designed to be located on the detector near to the pixel ROCs. In the case of the barrel, they will be mounted on the detector modules and will control the readout of 8 or 16 ROCs depending upon the layer radius. In the case of the forward disks, they will be mounted on the disk blades and will control the readout of 21 or 24 ROCs depending on blade side. A TBM and the group of ROCs that it controls will be connected to a single analog optical link over which the data will be sent to the Front End Driver, a flash ADC module located in the electronics house. The principle functions of the TBM include the following.

- It will control the readout of the ROCs by initiating a token pass for each incoming Level 1 trigger.
- On each token pass, it will write a header and a trailer word to the data stream.
- The header will contain an 8bit event number and the trailer will contain 8bits of error status. These will be transferred as 2bit analog encoded digital.
- It will distribute the Level 1 triggers, and clock to the ROCs.

Each arriving Level 1 trigger will be placed on a 32deep stack awaiting its associated token pass. Normally the stack will be empty but is needed to accommodate high burst rates due to noise, high track density events, or trigger bursts. Since there will be two analog data links per module for the inner two layers of the barrel, the TBMs will be configured as pairs in a Dual TBM Chip. In addition to two TBMs, this chip also contains a Control Network. The Hub serves as a port addressing switch for control commands that are sent from the DAQ to the frontend TBMs and ROCs. These control commands will be sent over a digital optical link from a Front End Controller (FEC) in the electronics house to the frontend hubs. The commands will be sent using a serial protocol, running at a speed of 40 MHz. This high speed is mandated by the need to rapidly cycle through a refreshing of the pixel threshold trim bits that can become corrupted due to single event upsets (SEU). There are four external, write only ports on each Hub for communicating with the ROCs and there is one internal read/write port for communicating with the TBMs within the chip. The first byte of each command will contain a 5bit hub address and a 3bit port address. When a Hub is addressed, it selects the addressed port, strips off the byte containing the hub/port address and passes the remainder of the command stream unmodified onto the addressed port. The outputs of the external ports consist of two low voltage differential lines for sending clock and data.

3.4 Analog chain

The hit information is read out serially through analog links in data packets containing all hits belonging to a single trigger. Within such packets a new analog value is transmitted every 25 ns and digitized in the Front End Driver (pxFED) a the same rate. Each pixel hit uses 6 values, or 150 ns. Five values are used to encode the address of a pixel inside a ROC and the sixth value represents the signal charge. Only the charge signals are truly analog while headers and addresses are discrete levels generated by DACs. No ROC IDs are sent but every ROC adds a header, whether it has hits or not in order to make the association of hits to ROCs possible. The sequential readout is controlled by a token bit which is emitted by the TBM, passed from ROC to ROC and back to the TBM. The differential electrical outputs of the ROCs are multiplexed by the TBM onto either one or two output lines. On the same lines the TBM transmits a header before starting the ROC readout. After receiving the token back from the

last ROC in the chain the TBM sends a trailer containing status information. From the TBM to the end ring of the pixel barrel the readout uses the module Kapton cable. The Kapton cable has a ground mesh on the back side and the differential analog lines are separated by quiet lines from the fast digital signals. Nevertheless, cross-talk from LVDS signals was found to be unacceptable and a low swing digital protocol is being used instead. On the end ring the analog signals are separated from the digital and all analog signals of the sector are sent on a separate Kapton cable to a printed circuit board that houses the Analog Optical Hybrids (AOH). The signal path between TBM and AOH is designed with a constant impedance of 40 Ohms and terminated on the AOH. The optical links of the pixel system are identical to those used in the strip tracker. An ASIC that adapts the output levels of the pixel modules to those expected by the laser driver has been added to the AOH of the pixel system. A clean identification of the six levels used for encoding pixel addresses is crucial for the reconstruction of hits. The ratio of RMS width to separation of the digitized levels after the full readout chain is 1:30. The rise-time at the digitizer input is 3 ns which makes corrections from previously transmitted levels negligible. The full readout chain adds a noise equivalent to 300 electrons to the analog pulse height, dominated by baseline variations of the laser drivers.

3.5 Front End Driver

Optical signals from the pixel front end electronics (ROCs and TBMs) are digitized using the Front End Digitizer (pxFED) designed by HEPHY Vienna and build as a 9U VME module. A pxFED module has 36 optical inputs each equipped with an optical receiver and an ADC. The ADC converts at LHC frequency supplied by the TTC system which can be adjusted by an individually programmed phase shift (16 steps within 25 ns) for precise timing. A programmable offset voltage to compensate bias shifts can also be set. The output of the 10bit-ADC is processed by a state machine to deliver pixel event fragments consisting of header, trailer, input channel number, ROC numbers, double column numbers and addresses and amplitudes of hit pixels all at a subject-dependent resolution of 5 to 8 bits. Event fragments are strobed into FIFO-1 (1k deep x 36bit wide) which can be hold on demand to enable read out via VME. In normal processing mode FIFO-1 is open and data of 4 (5) combined input channels are transmitted to 8 FIFO-2 memories (8k x 72bits). In order to determine thresholds and levels required for the state machine, FIFO-1 can alternatively be operated in a transparent mode making unprocessed ADC output data available.The output from FIFO-2 is clocked into two FIFO-3 memories (8k x 72bits) which outputs are combined to provide the data now at a frequency of 80MHz (twice the common operating pxFED-frequency) to the S-Link interface acting as a point-to-point link with the CMS-DAQ system. Parallel to the data flow spy FIFOs are implemented (restricted in size) to hold selected event fragments and make them available for checking data integrity. Error detection takes place in the data stream from FIFO-1 to FIFO-2 and corresponding flags are embedded in the event trailer and also accessible from VME. A selected DAC output from each ROC (on default representing the ROC's temperature) is available as well. In addition, errors are directly transmitted to the CMS-TTS system using a dedicated connector on the S-Link supplementary card. A histogramming feature has been implemented to monitor the rate of double column hits. This histogram is intended to be read out via VME periodically to check for dead or overloaded columns. The pxFED houses an internal test system which, when enabled, replaces the normal ADC input by a pattern of 256 clocked analog levels simulating a normal pixel event. There are three test DACs (10bit) available to generate such a pattern meaning that every third input channel receives the same simulated event. This test system allows to test most of the features of the pxFED without the need of external optical input signals. All FIFOs, the state machine with its adjustable parameters, the VME protocol, error detection and histogramming features are integrated into several FPGAs mounted on daughter cards making the pxFED flexible to changes and improvements. The corresponding firmware can be downloaded via VME or using a JTAG bus connector mounted on the mother board. The whole pixel readout system will consist of 40 pxFED modules (32 for the barrel and 8 for the forward) set up in three 9U VME crates located in the electronics room. Individual modules can be accessed by VME geographical addressing.

3.6 Front End Controller

Pixel Front End Controller (pFEC) supplies clock and trigger information to the front end, and provides a data path to the front end for configuration settings over a fiber optic connection. The pFEC uses the same hardware as the standard CMS FEC-CCS, with the firmware which defines the behavior of the mezzanine FEC (mFEC) module replaced, converting the FEC into a pFEC. Each mFEC board becomes two command links to the front end. The Trigger Encoder Performs all trigger transmission functions, Re-encoding TTC triggers to match the pixel standard, block triggers to a given channel, generate internal triggers, either singly, or continuously, for testing purposes. Within each command link are a one kilobyte output buffer for data transmission, and a two kilobyte input buffer for data receiving. All data, whether write or read operations, are retransmitted back from the

front end for possible verification. To minimize the VME data transfer time, the pFEC uses several data transfer modes. When transferring pixel trim values to the front end, the pFEC calculates the row number information for a given column of pixels on the fly. This results in nearly a 50% reduction in the time required to transfer trim values over VME to a given command link buffer. In this way, the entire pixel front end trims can be reloaded in 12 seconds. Another 2 seconds are used to load the other configuration registers, for a total of 14 seconds to reload the front end completely. This column mode is also the reason that the return buffer is twice as big as the transmit buffer. The return buffer receives the row number as well as the trim value for each pixel. Once data is loaded into an output buffer, the transfer may be initiated either by computer control, or by a signal from the TTC system. Since single event upsets are expected to occur in the front end registers, it is anticipated that periodic updates will be necessary. Since updating the front end may disrupt data taking, it is preferable to perform small updates synchronized to orbit gaps or private orbits. This is down through the TTC initiated downloads. For transmission verification purposes, the number of bytes transmitted is compared to the number of bytes returned from the front end. Also, the returning Hub/Port address is compared to the transmitted address. Status bits are set with the results of this comparison, and these values are stored, for possible review, should an error condition occur.

3.7 CCU system

The CMS Pixel detector front end control system for both the Barrel (BPix) and the Forward (FPix) detectors consists of four communication and control unit boards (CCU Boards). Each CCU board controls a quarter of the detector with eight Barrel readout sectors or twelve Forward port cards. Figure 4 shows the block diagram of a CCU Board. The same ring topology configured as a local area network as in the CMS tracker is used. The front end controller (FEC) module (see: Ref FEC) is the master of the network and uses two optical fibers to send the timing and data signals to a number of slave CCU nodes, and another two fibers to receive return communication traffic. The two receiver channels on the digital optohybrid (DOH) transmit the 40 MHz clock and control data at 40 Mbit/s in the direction from the FEC to the ring of communication and control units (CCUs). The two transmitter channels send clock and data back to the FEC from the ring of CCUs. The CCU is the core component developed for the slow control, monitoring and timing distribution in the tracking system [**?**]. To improve system reliability against a single component failure a redundant interconnection scheme based on doubling signal paths and bypassing of faulty CCUs is implemented. An additional "dummy" CCU node allows to mitigate a single DOH failure preserving complete functionality. A CCU node failure leads to a loss of communication to all electronics attached to that CCU. The first two CCU nodes in the ring provide also the I^2C data channels necessary to control the digital optohybrids on the CCU boards.

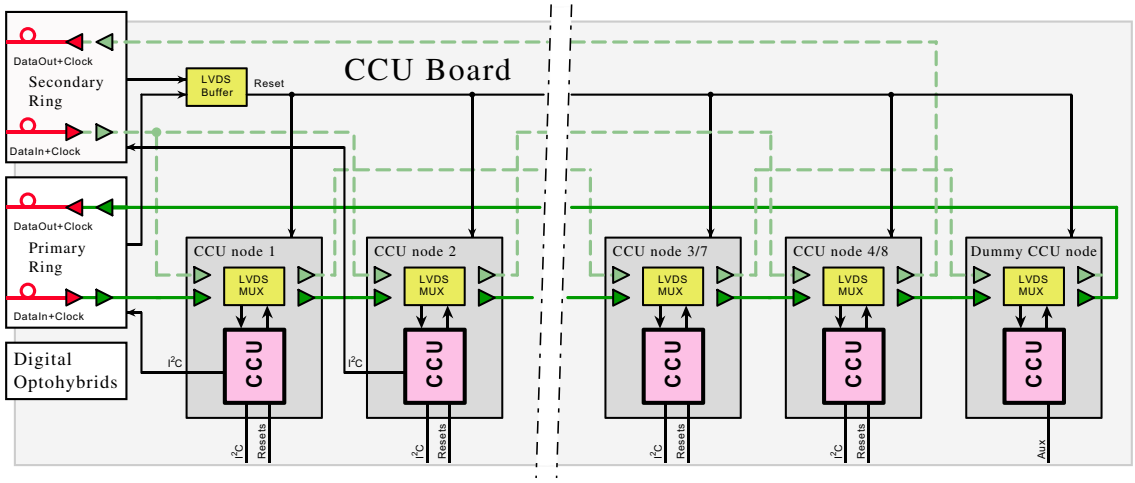

Figure 4: Block diagram of the Pixel front end control system. Note that the total number of CCU nodes is 9 for the BPix and 5 for the FPix.

In the BPix each readout sector is controlled by a separate CCU node. Eight active and one dummy CCU node build a single control ring. One I^2C data channel is used to access and control the front end readout electronics and three output channels generate the necessary signals to reset the digital and the analog optohybrids as well as the readout chips (ROCs) in one readout sector. The FPix control ring consists of four active and one dummy CCU node. Each of the active CCU nodes control 3 Port cards, which constitute a 45° sector in the detector coverage at one end. A connection between a CCU and a Port card includes a bi-directional 100 KHz I^2C communication

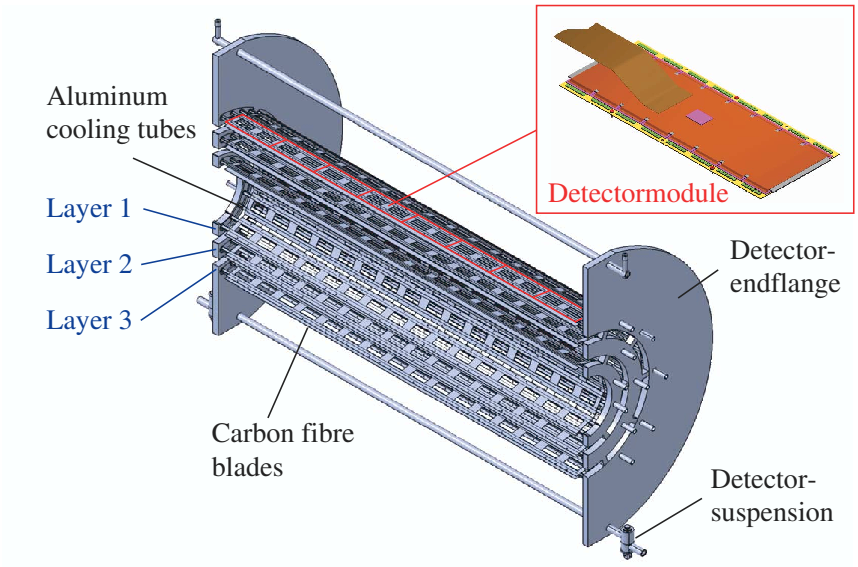

Figure 5: *Complete support structure half shell with the three detector layers.*

channel and two reset signals. One reset signal is for the Port card electronics, and the other one goes to the readout chips on the detector panels.

4 The pixel barrel system

The pixel barrel system as installed inside CMS comprises the barrel itself, i.e. detector modules mounted on the their cylindrical support structure, as well as supply tubes on both sides. The barrel with its length of 57 cm is much shorter than the strip tracker inside of which it is installed. Supply tubes carry services along the beam pipe from patch panels located outside of the tracker volume to the barrel. The supply tubes also house electronics for readout and control. The length of the full system is 5.60 m. Support structure and supply tubes are split vertically to allow installation in the presence of the beam-pipe and its supports. Electrically the +z and -z sides of the barrel are separated. Each side is divided in 16 sectors which operate almost independently, sharing only the slow control system.

4.1 Pixel Barrel support structure

The detector support structure for the three layers at the radii of four, seven and eleven centimeters equipped with silicon pixel modules has a length of 570 mm ranging from -285 mm to +285 mm closest to the CMS interaction point. Fig. 5 shows a sketch of a complete support structure half shell.

Aluminum cooling tubes with a wall thickness of 0.3 mm are the backbones of the suppport structure. Carbon fiber blades with a thickness of 0.24 mm are glued onto the top or bottom two adjacent cooling tubes in such a way that their normal directions alternate pointing either to the beam or away from it. The tubes have trapezoidal cross sections defined by the azimuthal angles of the ladders they hold.

Four to five of these tubes are laser welded[12] to an aluminum container which distributes the cooling fluid. The resulting manifold provides the necessary cooling of the detector modules to about -10 °C with C_6F_{14}. Support frames on both ends, which connect the single segments, build a complete detector layer half shell. These flanges consist of thin fibreglass frames (FR4) that are filled with foam (Airex, [13]) and covered by carbon fibre blades.

Printed circuit boards mounted on the the flanges hold the connectors for the module cables and provide control signal fan-out and power distribution to the individual modules of a sector.

4.1.1 Pixel Detector Supply Tube

The electrical power lines, the electrical control signal and the optical signals as well as the cooling fluid are transferred across the supply tubes to the pixel barrel. The two supply tube parts of a half shell in +z and -z

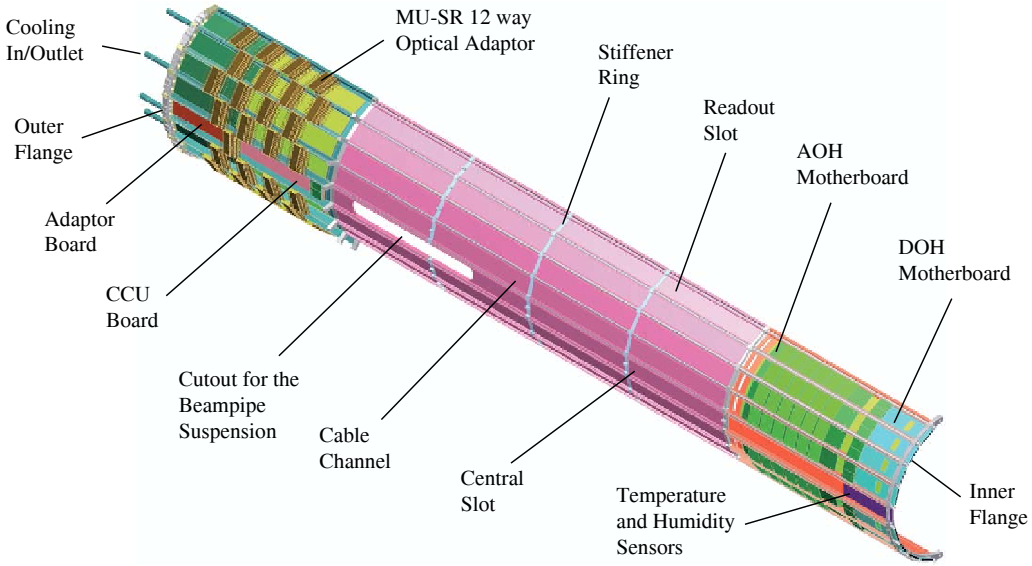

Figure 6: *Overview of a supply tube half shell.*

direction have a length of 2204 mm (see Fig. 6).

The supporting elements of the basic structure are the stainless steel tubes with a wall thickness of 0.1 mm running along the z-direction connected to the stiffener rings (FR4) and the inner and outer flanges made out of aluminum. The Tubes supply the detector with the cooling fluid. The gaps in between are filled with foamed material (Airex, [13]) with the corresponding shape to guarantee the necessary rigidity. All power and slow control leads are embedded in the supply tube body. This allows a clear layout of the wiring and makes the system also more reliable.

The motherboards, which hold the optical hybrids for the analog and digital control links, are installed in the eight readout slots near the detector on the integrated supply boards. The correspondig boards at the outer ends carry the power adaptor boards, which provide the detector power and the bias voltage for this sector. In the central slot the digital communication and control board (CCU Board (see: Ref CCUBoard)) is installed . From here the digital control signals are distributed to the individual readout boards in each of the eight readout sectors. Here also all slow control signals like temperatures, pressures and the humidity are brought together and connected by the dedicated slow control adaptor board to the cables. The optical fibres are installed in the cable channels. The 36 single fibres for the analog readout and the eight fibres for the digital control of the detector modules will then be connected through the MUSR connector to the optical ribbon cable. These adaptors are mounted at the circumference in the first part of the supply tube. The length of each supply tube is 2204 mm. Only a flexible mechanical connection is made between the barrel and the supply tube.

4.2 Pixel Barrel Detector Modules

The barrel part of the CMS pixel detector consists of about 800 detector modules. While the majority of the modules (672) are full modules as seen in Fig.7 on the right, the edges of the six half-shells are equipped with 16

half-modules each (96 in total, see Fig.7 on the left).

4.2.1 Geometry and Components

A module is composed of the following components (Fig. 7): One or two basestrips made from 250 μm thick silicon nitride provide the support of the module. The frontend electronics consists of 8 to 16 readout chips based on IBMs 0.25 μm deep-submicron process with 52x80 pixels of size 150x100 μm^2 each, which are bumpbonded to the sensor, a n-on-n device with moderated p-spray made from 285 μm thick DOFZ-silicon in $< 111 >$ orientation. The High Density Interconnect, a flexible low mass 3 layer PCB with a trace thickness of 6 μm equipped with a Token Bit Manager chip that controls the readout of the ROCs, forms the upper layer of a module and distributes signals and power to the chips. The signals are transferred over an impedance matched 2 layer Kapton/copper compound cable with 21 traces and 300 μm pitch. The module is powered via 6 copper coated aluminum wires of

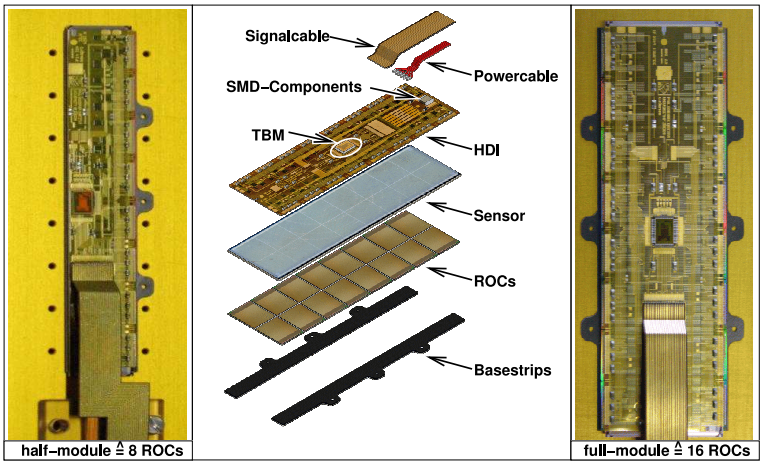

Figure 7: Exploded view (middle) of a barrel pixel detector fullmodule (right) and picture of an assembled half-module (left)

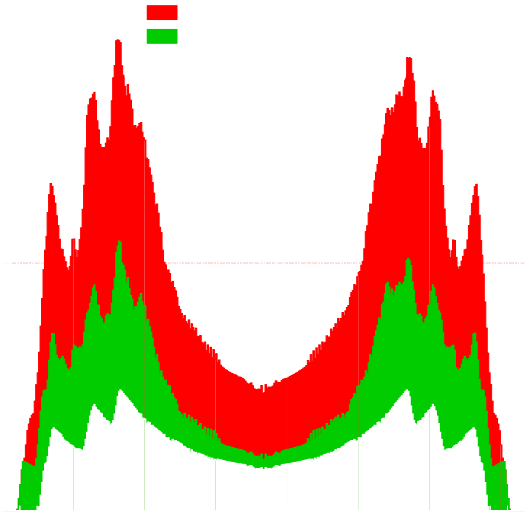

Figure 8: Material budget of the pixel barrel in units of radiation length versus rapiditiy.

250 μm diameter.

A completed full-module has the dimensions 66.6x26.0 mm^2, weight 2.2 g plus up to 1.3 g for cables, and consumes 2 W of power. The material of the pixel barrel amounts to 5 percent of a radiation length in the central region.Sensors and readout chips contribute one third of the material while support structure and cooling fluid contribute about 50 percent. The distribution of material as a function of pseudo-rapidity is shown in Fig. 8.

4.2.2 Assembly

With a sequence of photolithographic steps, UBM sputtering and indium evaporation and a final liftoff step the sensor- and ROC-wafers are prepared for the bumpbonding process. The ROC wafers are then thinned down to 170 μm and ROC- and sensor-wafers are diced and picked based on the results of acceptance tests. Finally the raw devices are cleaned and tested again. Only chips with less than 1% statistically distributed dead or noisy pixels and without pixel masking defects are used in the following assembly steps. A sensor is discarded when either the dark current is above 2 μA at 150 V and room temperature or the ratio of the dark currents measured at 100 V and 150 V is greater than two.

Sensor and ROCs are bumpbonded using the automatic bump-bonding machine developed at PSI. The individual ROC chips are tested during the bump-bonding process to ensure that only electrically working chips are bump-

bonded to the sensor. To form a mechanical and electrical connection between the indium bumps of sensor and ROCs the module is reflowed in the reflow oven. Afterwards the completed raw module is tested again and a reworking step to remove defective chips or improve the bump yield is done if needed. The overall chip replacement yield is about 85%.

The module assembly is completed by glueing the basestrips and the HDI, which is assembled with power and signal-cable and the TBM-chip and tested before. Wirebonding the ROCs to the HDI finalises the module assembly and a final test including thermal cycling is conducted. Details on the module assembly can be found in [14].

4.3 Qualification Procedures of the CMS Pixel Barrel Modules

The test procedure is divided into three main steps: Initialization, functionality tests and qualification / calibration procedures [15]. During the first step, the module has to be set up, so that the functionality tests can be performed in a controlled way. This includes setting the analog current of each readout chip to a common value, adjusting the timing of the internal calibration signal, tuning the signal threshold and the various levels of the analog output signal. In the second step the basic functionalities of all pixels are tested. Each pixel is required to have a full readout efficiency and its address must be decoded correctly. Furthermore the trim mechanism of each pixel has to be functional. In a newly developed, purely electrical test the connection of each readout chip pixel to its corresponding sensor pixel is verified. In the last step several qualification and calibration tests are executed. One of these is the measurement of the sensor $I-V$ curve up to 600 V. For each pixel, the noise and the dependency of the pulse height as a function of the injected charge is determined. At the end the trim algorithm unifies the thresholds of all pixels. The whole test procedures are performed at $+17°$C and $-10°$C. The module is thermal cycled 10 times between these two temperatures. All together, the qualification procedure take 9 to 10 hours per module. Based on all the data collected during the tests, each module is graded in one of three categories. Modules with less than 1% defective pixels are designated for use in the final system. Modules with more than one but less than 4% are spare modules, modules with more defective pixels are not going to be used. Defective pixels not only include non-responsive pixels, but also pixels which are noisy, badly bump bonded, etc. Various other grading criteria, e.g. on the $I-V$ curve or the pulse height calibration, are used. So far a yield of 82% for good and spare modules together was obtained.

5 Cooling

The power consumption per pixel amounts to around 50μW, including about 13 μW from the sensor leakage current at final fluences of 6×10^{14}/cm^2. For the total of $\approx$ 75 million pixels this adds up to 3.75 kW. The power load on the Aluminum cooling tubes is therefore expected to be about 50 W/m. The sensor temperature will be maintained at around -10°C. As for the strip detectors, liquid phase cooling with C_6F_{14} fluorocarbon is used. To keep the temperature increase of the coolant below $2°$, a total flow rate of 1 litre/sec is required.

The pixel system is cooled by a total of 18 cooling loops: 10 for the barrel and 4 for each of the two end disk systems. For the barrel, the coolant enters at +z and exits at -z, or vice versa. The coolant for the two disk sets on each side of the interaction region is supplied and reclaimed from the same z side. One barrel loop feeds in parallel 9 thin-walled Aluminum pipes, each cooling 8 modules in series. One disk loop cools in parallel one quarter of each of the 3 disks; inside the quarter disks the 6 blade loops are connected serially. The coolant flow at the pixel modules is turbulent. The total lengths of the cooling loops starting from and returning to the pixel cooling rack amount to about 80 m, resulting in pressure drops of below 2 bar.

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